DESCRIPTION

SEMICONDUCTOR MEMORY DEVICE

5

Technical Field

The present invention relates to a

10 semiconductor memory device, and in particular,

relates to a semiconductor memory device having a

redundancy circuit that conducts a repair of a

defective memory cell.

15 Background Art

In a manufacturing process of a semiconductor

memory, a defect is generated on a chip, caused by

dust on a surface of a wafer, uneveness in abrasive

in polishing the surface of the wafer, and so on.

20 When a small defect is generated on a chip, the chip

itself is regarded as a defective product although

only a memory cell having the defect portion is

defective and other portions operate normally. It is

possible to improve a manufacturing yield by

25 providing a spare memory cell on the chip of the

semiconductor memory and replacing read/write data

for a defective memory cell with data for the spare

memory cell. For this reason, it has become popular
with the increase in the capacity of the
semiconductor memory to provide a redundancy circuit
that contains a spare memory cell and a control

5 circuit.

Relationships between a memory cell and a
spare memory cell on a chip are now explained with
reference to Fig. 1. As shown in Fig. 1A, a memory
block 71 has segments 71-0, 71-1, …. A segment is a

10 unit which is designated for repairing a defective
memory cell when a defect is generated. A redundancy
memory block 72 has redundancy segments 72-0 and 72-1
that substitute for the segments including the
defective memory cells. When a size of a defect 75

15 generated in the memory block 71 is small, the defect
75 fits into only the single segment 71-0 of the
memory block 71, as in the case of an example shown
in Fig. 1A. Information stored in a memory cell
group associated with the defect 75 is repaired by

20 the redundancy segment 72-0 in the redundancy memory
block 72.

However, as a process scale is miniaturized
year by year and the size of the memory cell is
reduced, the size of the defect becomes relatively

25 larger in comparison with the size of the memory cell,
as shown in Fig. 1B. As a result, the defect does
not fit into a single segment but is generated over

adjacent successive segments. For this reason, even when the defect 75 having the same size as the defect shown in Fig. 1A is generated, three segments from the segments 73-0 to 73-2 are defective in the

5 example shown in Fig. 1B. Therefore, a redundancy memory block 74 that repairs the defect needs three or more redundancy segments. As described above, a single redundancy segment can repair the defect 75 in the example shown in Fig .1A. However, in the

10 present day when the process is miniaturized, three redundancy segments are necessary, and defective memory cells concentrates on a specific memory block and is unevenly distributed, as shown in Fig. 1B.

On the other hand, a defective address

15 indicating a memory cell group associated with the defect 75 is held by a redundancy circuit. A fuse is often used for holding the defective address. In the case of Fig. 1A, the fuse holds an address indicative of the segment 71-0 as the defective address. When

20 the memory block 71 is accessed, and when the defective address held by the fuse matches an access address, the segment 72-0 in the redundancy memory block 72 is accessed.

In recent years, address information of a

25 memory is increased due to the increase in the memory capacity. As mentioned above, a capacity of the redundancy memory itself also has to increase. The

increase in the capacity of the redundancy memory leads to an increase in the number of fuses which hold the defective addresses.

5   A configuration of a conventional redundancy memory is described with reference to Fig. 2. As shown in Fig. 2, a system has sub mats 81-0 to 81-7, a sub mat decoder 82 and a column decoder 83, where a redundancy circuit is provided for every sub mats. In general, redundancy circuits are provided in both

10   a row side and a column side. For simplification of the explanation, only the row side is represented in Fig. 2, and the redundancy circuit in the row side will be explained. Here, an address X0 to X13 of 14 bits is inputted as a row address. The address X11

15   to X13 is used for selecting one of the eight sub mats. The address X3 to X10 is used for selecting one of 256 main word lines MWD of the selected sub mat. The address X0 to X2 is used for selecting one of eight sub word lines SWD. Since eight sub word

20   lines SWD are related to one main word line MWD with regard to word lines, each of the sub mats has 2048 word lines in total (the 256 main word lines × the eight sub word lines). Thus, Fig. 2 shows a memory that has eight spare word lines for the 2048 word

25   lines in each of the sub mats.

The sub mats 81-0 to 81-7 are selected by sub mat selection signals SM0 to SM7 generated by the sub

mat decoder 82, respectively. The sub mat 81-0 is
provided with a memory cell array 85-0 which is a
memory block, a row address decoder 86-0, a
redundancy memory cell array 87-0 which is a

5 redundancy memory block, a redundancy row address
decoder 88-0, redundancy ROM circuits 91-0-0 to 91-0-
7, a sub word decoder 89-0, an AND circuit 93-0, and
an OR circuit 94-0. It should be noted that
additional numbers attached to reference numerals are

10 given to make a distinction between similar
components, and are omitted when the distinction is
not necessary. Also, the other sub mats 81-1 to 81-7
have the same configuration as the sub mat 81-0. The
only difference is that respective of SM1 to SM7 are

15 inputted as the sub mat selection signals SM.
Therefore, description will be given only on the sub
mat 81-0, and explanation of the other sub mats 81-1
to 81-7 will be omitted.

In the sub mat 81-0, the memory cell array

20 85-0 is a group of memory cells of a main body. A
memory cell row connected to a word line selected by
the row address decoder 86-0 and the sub word decoder
89-0 is activated, and data of the memory cell is
amplified by a sense amplifier 84-0. Further, a

25 sense amplifier is selected by a column address
decoder 83, and the data is transmitted to an I/O
circuit (not shown).

The row address X3 to X10 is inputted to the row address decoder 86-0. The inputted row address is decoded, and one of the 256 main word lines MWD is selected and activated. The sub word decoder 89-0

5 receives the row address X0 to X2, selects one of the eight sub word lines SWD, and activates the sub word line SWD connected to the activated main word line MWD. Thus, one of the 2048 word lines is activated by the row address decoder 86-0 and the sub word

10 decoder 89-0.

The redundancy memory cell array 87-0 is a redundancy memory for repairing a defective portion of the memory cell array 85-0. A redundancy main word line RMWD in the redundancy memory cell array

15 87-0 is activated by the redundancy row address decoder 88-0.

The redundancy row address decoder 88-0 decodes a row address in the redundancy memory cell array 87-0. Redundancy selection signals RE

20 outputted from the redundancy ROM circuits 91-0-0 to 91-0-7 is inputted to the redundancy row address decoder 88-0, and a redundancy main word line RMWD is activated. Thus, the redundancy row address decoder 88-0 activates the redundancy main word line RMWD,

25 when any of the redundancy selection signals RE-0-0 to RE-0-7 is activated.

The redundancy ROM circuits 91-0-0 to 91-0-7

hold defective addresses which indicate positions of the defects in the memory cell array 85-0 to be replaced, and determines whether the redundancy memory cell array 87-0 is selected or not. When the redundancy memory cell array 87-0 is selected, the redundancy selection signal RE is activated. With respect to the defective addresses in the memory cell array 85-0, address information corresponding to the row address X0 to X10 are programmed in fuses provided to the redundancy ROM circuits 91-0-0 to 91-0-7. When the memory cell array 85-0 is accessed, the redundancy ROM circuits 91-0-0 to 91-0-7 compare the address information programmed in the fuses with the row address X0 to X10 to be accessed. In a case of match as a result of the address comparison, the redundancy ROM circuits 91-0-0 to 91-0-7 determines that the row address to be accessed is the defective address, and activates the redundancy selection signal RE. In a case of mismatch as a result of the address comparison, the memory cell array of the main body is to be selected, and the redundancy selection signal RE is not activated.

The sub word decoder 89-0 decodes the lower bits X0 to X2 of the row address, activates a sub word line SWD connected to the main word line MWD activated by the row address decoder 86-0, and activates the word line of the memory cell row to be

accessed. When a defective address is accessed, the redundancy memory cell array 87-0 instead of the memory cell row specified by the row address should be accessed. It is therefore necessary to invalidate

5   the row address inputted to the sub word decoder 89-0, and to access the redundancy memory cell array 87-0 in accordance with the redundancy selection signal RE outputted from a redundancy ROM circuit holding the defective address among the redundancy ROM circuits

10 91-0-0 to 91-0-7. For this reason, the sub word decoder 89-0 receives the redundancy selection signals RE-0-0 to RE-0-7 outputted from respective of the redundancy ROM circuits 91-0-0 to 91-0-7. When any of the redundancy selection signals RE-0-0 to RE-

15 0-7 is activated, the sub word decoder 89-0 switches a selector of the sub word decoder 89-0 by using an output of the OR circuit. Also, the sub word decoder 89-0 outputs the redundancy selection signal RE as a signal for selecting the redundancy sub word line

20 RSWD instead of a signal obtained by decoding the lower three bits of the row address.

The AND circuit 93-0 generates a redundancy activation signal BE for activating the redundancy ROM circuits 91-0-0 to 91-0-7. A logical

25 multiplication of the sub mat selection signal SM0 indicating that the sub mat 81-0 is selected and an access activation signal AE indicating that the

memory cell is to be accessed is a condition for
activating the redundancy ROM circuits 91-0-0 to 91-
0-7.

5   The OR circuit 94-0 receives the redundancy
selection signals RE-0-0 to RE-0-7 outputted from the
redundancy ROM circuits 91-0-0 to 91-0-7, and outputs
a logical addition thereof as a row address decoder
killer signal XDK. The row address decoder 86-0 gets
into an inactive state, in response to the row
10   address decoder killer signal XDK. Consequently, the
memory cell array 85-0 is not activated.

Normal memory access in the above
configuration is performed as follows. Here, an
operation to read out data stored in the memory cell
15   is explained.

When an access address and an instruction to
read data are given, the row address X0 to X13 is
validated and the access activation signal AE is
activated. The upper row address X11 to X13 is
20   inputted to the sub mat decoder 82, and one of the
sub mat selection signals SM0 to SM7 which selects
any of the sub mats 81-0 to 81-7 to be accessed is
activated. When the row address X11 to X13 is all
zero, the row address indicates that the sub mat 81-0
25   is to be accessed, and the sub mat selection signal
SM0 is activated. When the sub mat selection signal
SM0 is activated, the AND circuit 93-0 takes the

logical multiplication of the access activation signal AE and the sub mat selection signal SM0 to activate the redundancy activation signal BE. The redundancy activation signal BE activates the

5 redundancy ROM circuits 91-0-0 to 91-0-7.

The redundancy ROM circuits 91-0-0 to 91-0-7 store states of the fuses in latch circuits beforehand, at the time of initial setting such as the time of the power activation. Information of the

10 defective addresses held in the latch circuits and the inputted row address X0 to X10 are compared in an address comparator.

In a case of mismatch as a result of the comparison, it is indicated that the memory cell at

15 the address to be accessed has no defect. Therefore, the memory cell array 85-0 is accessed, and the redundancy selection signal RE is not activated. Unless any of the redundancy ROM circuits 91-0-0 to 91-0-7 is activated, the row address decoder killer

20 signal XDK is not activated, and one main word line MWD selected by the row address decoder 86-0 is activated. Similarly, in the sub word decoder 89-0, the output of the OR circuit is not activated, and one sub word line selected based on the row address

25 X0 to X2 is activated. A memory cell row 80 is activated which is connected to a word line selected in accordance with decoding results in the row

address decoder 86-0 receiving the row address X3 to X10 and the sub word decoder 89-0 receiving the row address X0 to X2. Data corresponding to the access address is outputted from the memory cell row 80

5   through the sense amplifier 84-0 selected by the column address decoder 83 to which a column address is supplied.

In a case of match as a result of the comparison, it is indicated that the memory cell at

10   the access address has a defect, and the redundancy memory cell array 87-0 is then accessed. To access the redundancy memory cell array 87-0, a redundancy ROM circuit 91 holding the defective address that matches the access address among the redundancy ROM

15   circuits 91-0-0 to 91-0-7 activates the redundancy selection signal RE. When the redundancy selection signal RE is activated, the OR circuit 94-0 activates the row address decoder killer signal XDK to inactivate the row address decoder 86-0.

20   Consequently, the memory cell array 85-0 is not accessed. The redundancy selection signals RE-0-0 to RE-0-7 are supplied to the redundancy row address decoder 88-0, and a redundancy main word line RMWD in the redundancy memory cell array 87-0 is activated.

25   Since one of the redundancy selection signals RE-0-0 to RE-0-7 inputted to the sub word decoder 89-0 is activated, the selector is switched. Outputted from

the sub word decoder 89 is not a signal which selects

a sub word line SWD in the memory cell array 85-0

corresponding to the decoding result of the row

address X0 to X2 but a signal which selects a

5   redundancy sub word line RSWD specified by the

redundancy ROM circuit 91-0.

A memory cell row 92 is activated that is

connected to the word line in the redundancy memory

cell array 87-0 selected by the redundancy sub word

10 line RSWD specified by the redundancy ROM circuit 91-

0. Data corresponding to the access address is

replaced by the data of the redundancy memory cell

array 87-0 and is outputted from the memory cell row

92 through the sense amplifier 84-0 selected by the

15 column address decoder 83 to which a column address

is provided.

In the case of the above example, the number

of the fuses holding the defective addresses is

eleven per one redundancy ROM circuit 91, which

20 corresponds to the row address X0 to X10 of 11 bits.

Also, eight row addresses can be replaced in one sub

mat. Therefore, if the defects are detected in 9 or

more row addresses in the one sub mat 81, the memory

chip cannot be repaired even if there is no defect in

25 the other sub mats 81.

Thus, it is necessary to efficiently conduct

a repair by using a redundancy circuit while reducing

the chip size by designing circuits dedicated to the redundancy circuit as less as possible. In a case where defects are evenly distributed over a memory block and between memory blocks, it is possible to

5 repair the defective cells by providing redundancy circuits, the number of which is determined stochastically. However, the repair of the defects generated in the memory block is limited by the number of redundancy circuits provided in the block.

10 There is a problem in that the memory chip cannot be repaired when the defective cells concentrate in a particular memory block and the number of addresses to be replaced exceeds the number of redundancy circuits.

15   Next, a flexible method is explained, which redeems the above-mentioned shortcomings and improves repair efficiency. According to the considered flexible method, a redundancy circuit is not provided for each memory block, but a larger redundancy

20 circuit is provided for a larger memory block. Although the fraction of redundancy circuit size per a memory block is the same, it is possible to repair the defects which are unevenly distributed, since an absolute number of the redundancy circuits handling

25 the memory block is increased.

       For example, the redundancy ROM circuit 91 shown in Fig. 2 is replaced by a redundancy ROM

circuit 96 shown in Fig. 3. The number of fuses holding the defective addresses is increased by three per a redundancy circuit in comparison with the circuit in Fig. 2, and the access address is compared with the row address X0 to X13. The access activation signal AE is directly supplied to the redundancy ROM circuit 91 such that it is activated whenever any of the sub mats 81-0 to 81-7 is accessed. Then, the redundancy ROM circuit 96 can be used in common in all sub mats 81. In Fig. 2, eight redundancy circuits are provided for each of the sub mats 81-0 to 81-7. According to the redundancy ROM circuit shown in Fig. 3, 64 redundancy circuits shared by respective of the sub mats 81-0 to 81-7 are provided. Thus, even if there are ten defective addresses to be replaced in the sub mat 81-0, the chip can be repaired if there are no defects at all in the sub mats 81-1 to 81-7.

As stated above, the number of fuses holding the defective addresses in the redundancy ROM circuit 96 is fourteen, which corresponds to the row address X0 to X13. Also, the number of defects that can be replaced with in one memory block is 64.

According to the flexible method, although the capability to repair the unevenly-distributed defects is improved, there is a problem that the number of fuses in the redundancy circuit is

increased due to the increase in the size of the memory block that is to be replaced.

The size of the fuse is approximately 3 times 60 micrometers, which is very large as compared with

5 the memory cell size being approximately 0.13 square micrometers. Therefore, the number of fuses should be as small as possible. For example, in a case when the memory is divided into 2^n memory blocks and m redundancy memory cell rows are provided to each of

10 the memory blocks, the number of the redundancy memory cell rows is $m \times 2^n$. When the bit number of the address which specifies the redundancy memory cell row is X, the number of fuses provided to the redundancy circuit is $(X-n) \times m \times 2^n$ in the former method,

15 and is $X \times m \times 2^n$ in the latter method. For example, as compared with a case where the memory is divided into eight (n=3) and eight redundancy circuits are provided in the former case, extra 192 fuses are necessary in the latter case.

20 As described above, it is important to reduce the number of fuses, as the memory capacity increases and the memory cell is miniaturized. A method which is the combination of the former and the latter methods is also known (e.g. Japanese Laid Open Patent

25 Application JP-P2001-143494A). According to the method, some of the redundancy circuits are allocated to a divided memory block, and the remaining

redundancy circuits are allocated to a plurality of division memory blocks.

Also, Japanese Laid Open Patent Application JP-A-Heisei 5-242693 discloses a technique, in which two column lines in a column direction are simultaneously replaced by a redundancy circuit, the redundancy circuit is composed of two redundancy blocks, two redundancy blocks are selected by lower column addresses, and a ROM circuit (a fuse and a program circuit) of the redundancy circuit is used in common to reduce the fuse area and selection circuit.

[Patent Document 1] Japanese Laid Open Patent Application JP-P2001-143494A

[Patent Document 2] Japanese Laid Open Patent Application JP-A-Heisei 5-242693

Disclosure of Invention

An object of the present invention is to provide a semiconductor memory device that is provided with a redundancy circuit performing a repair of a defective memory cell and can efficiently repair unevenly-distributed memory cell failures.

Another abject of the present invention is to provide a semiconductor memory device having a redundancy circuit in which the number of fuses holding information of defective addresses is reduced.

Also, another object of the present invention

is to provide a semiconductor memory device having a redundancy circuit in which an occupied area of fuses holding information of defective addresses is reduced.

Further, another object of the present
5 invention is to provide a semiconductor memory device that can repair defective memory cells which are unevenly distributed and improve the yield.

In an aspect of the present invention, a semiconductor memory device having a redundancy
10 circuit is provided with a plurality of memory blocks and a plurality of redundancy memory blocks provided for each of the plurality of memory blocks. An address bit for selecting each of the plurality of memory blocks is different from an address bit for
15 selecting each of the plurality of redundancy memory blocks.

In the semiconductor memory device of the present invention, one or more adjacent memory cell rows or columns owned by each of the plurality of
20 memory blocks is referred to as a segment which is a unit of allocation as a replacement target. Adjacent segments having defects are replaced by redundancy segments respective of which are provided in different ones of the plurality of redundancy memory
25 blocks.

In the semiconductor memory device of the present invention, address bits that define the

segment are lower address bits. Address bits for selecting the plurality of redundancy memory blocks include an address bit immediately above the lower address bits.

5   In the semiconductor memory device of the present invention, a unit of the segment is equal to the number of sub word lines.

In another aspect of the present invention, a semiconductor memory device has a memory block and a
10 plurality of redundancy memory blocks. The memory block has a plurality of segments, and each of the plurality of segments is provided with a plurality of memory cells. The plurality of redundancy memory blocks are provided for the memory block. Each of
15 the plurality of redundancy memory blocks has a redundancy segment. The redundancy segment substitutes for any segment having a defect of the plurality of segments. The plurality of segments are cyclically and sequentially allocated to the
20 plurality of redundancy memory blocks. When having a defect, each of the plurality of segments can be replaced by the allocated redundancy memory block.

In another aspect of the present invention, a semiconductor memory device has a plurality of memory
25 blocks and a plurality of redundancy memory blocks. Each of the plurality of memory blocks has a plurality of segments, and each of the plurality of

segments has a plurality of memory cells. The

plurality of redundancy memory blocks are provided

for the plurality of memory blocks. Each of the

plurality of redundancy memory blocks has a

5 redundancy segment. The redundancy segment

substitutes for any segment having a defect of the

plurality of segments. The plurality of segments are

cyclically and sequentially allocated to the

plurality of redundancy memory blocks. When having a

10 defect, each of the plurality of segments can be

replaced by the allocated redundancy memory block.

In another aspect of the present invention,

in a semiconductor memory device having a plurality

of memory blocks, each of the plurality of memory

15 blocks includes a plurality of segments. A

redundancy memory block, which substitutes for any

segment having a defect of the plurality of segments,

is physically provided to each of the plurality of

memory blocks. The redundancy memory block is

20 logically allocated to the plurality of memory blocks

in common. When having a defect, each of the

plurality of segments can be replaced by the

allocated redundancy memory block.

In the semiconductor memory device of the

25 present invention, a first segment and a second

segment of the plurality of segments are adjacent to

each other. A first redundancy memory block

allocated to the first segment and a second redundancy memory block allocated to the second segment are different redundancy memory blocks.

In the semiconductor memory device of the present invention, an address indicating the first segment and an address indicating the second segment are successive addresses. A number indicating the first redundancy memory block and a number indicating the second redundancy memory block are cyclically successive.

According to the semiconductor memory device of the present invention, when k is a number indicating the redundancy memory block allocated to any of the plurality of segments, m is an address indicating any of the plurality of segments, and n is the number of the plurality of redundancy memory blocks, the k is given by a remainder generated when the m is divided by the n.

In the semiconductor memory device of the present invention, each of the plurality of segments is a group of memory cells connected to 2^n (n=0, 1, 2,...) word lines or bit lines. When the number of the word lines or the bit lines is plural, the word lines or the bit lines are adjacent.

In the semiconductor memory device of the present invention, a plurality of lower bits of an address inputted to a decode circuit for selecting

any of the plurality of segments are also inputted to a decode circuit for selecting any of the plurality of redundancy memory blocks.

According to the present invention, it is
5 possible in a semiconductor memory device provided with a redundancy circuit performing a repair of a defective memory cell to efficiently repair unevenly-distributed memory cell failures.

Also, according to the present invention, it
10 is possible to provide a semiconductor memory device having a redundancy circuit in which the number of fuses holding information of defective addresses for specifying defective memory cells is reduced.

Further, according to the present invention,
15 it is possible to provide a semiconductor memory device having a redundancy circuit in which an occupied area of fuses is reduced, since the number of the fuses holding the information of the defective addresses for specifying the defective memory cells
20 is reduced.

Additionally, according to the present invention, it is possible to repair unevenly-distributed defective memory cells by dispersing the redundancy circuits and to improve yield of the
25 semiconductor memory device.

Best Mode for Carrying Out the Invention

A semiconductor memory device according to a first embodiment of the present invention will be described with reference to Figs. 4 to 9. In general, a semiconductor memory device (DRAM) has a redundancy circuit in one of or each of a row side and a column side. In order to simplify the description, the redundancy in the row side will be described below. It is obvious that the present invention is applicable to the redundancy in the column side as well.

In the first embodiment, a segment which is a unit for replacing a defect is a memory cell group connected to one word line selected by a row address. In the present invention, the memory cell group connected to the one word line is referred to as a sub memory block. Therefore, the size of the segment and that of the sub memory block are equal in the first embodiment.

In the first embodiment, memory cell arrays are allocated in a mosaic form to redundancy memory cell arrays. A repair is possible even if failing bits are generated to concentrate on a specific block, and the number of fuses in a redundancy selection circuit is reduced. In other words, redundancy sub memory blocks for unevenly-distributed failures are distributed over the redundancy memory cell arrays. In the conventional technique, the repair may be

impossible due to a shortage of the redundancy sub memory blocks when the failing bits are generated with a concentration. According to a configuration of the present embodiment, however, the repair is

5   possible because the sub memory blocks of failing bit group are dispersively allocated to the redundancy memory cell arrays. Such a configuration or method is referred to as a mosaic segment redundancy, since the sub memory blocks in the memory cell array are

10   allocated to the redundancy memory cell arrays in a mosaic form.

Fig. 4 is a block diagram showing a configuration of a 1G bit DRAM provided with a redundancy ROM circuit. A DRAM chip 10 has a control

15   circuit 11, an I/O circuit 12 and banks 14-0 to 14-7. Here, reference numerals with hyphens and additional numbers attached denote the same configurations, and the hyphen and the additional number are omitted when distinction is not particularly necessary.

20   The control circuit 11 is a circuit for controlling an operation of the DRAM. The control circuit 11 analyzes an input command, outputs a timing signal and a control signal to each section, and performs a normal memory operation corresponding

25   to the command.

The I/O circuit 12 receives an external address signal indicative of a data location, and

writes data indicated by a data signal to a memory
cell indicated by the address signal, or outputs data
read from the memory cell at the address as a data
signal.

5   The bank 14 is a unit in which the memory
cell array of each of the banks can be independently
activated. The DRAM shown in Fig. 4 has an eight-
bank configuration of the banks 14-0 to 14-7. The
bank 14 is divided into some sections and controlled.
10 The divided memory cell assembly is referred to as a
mat. In the case of Fig. 4, each of the banks 14 is
divided into four sections and has mats 16-0 to 16-3.

          The mat 16 is further divided into some
sections and controlled. The divided memory cell
15 assembly is referred to as a sub mat. In the case of
Fig. 4, one mat 16 has eight sub mats 17-0 to 17-7.
A column address decoder 18 for decoding a column
address (Y address) and an I/O circuit 19 for
inputting and outputting data are provided in common
20 to the sub mats. One sub mat is selected from the
sub mats 17-0 to 17-7 by using the upper three bits
(X11 to X13) of a row address (X address).

          The sub mat 17 is a unit having a memory cell
array group surrounded by a row address decoder 22
25 and a sense amplifier 25 (including column SW). The
sub mat 17 has a memory cell array 21, the row
address decoder 22, a redundancy memory cell array 23,

a redundancy row address decoder 24, and the sense
amplifier 25.

Fig. 5 is a block diagram showing a
configuration of the sub mat 17 and the periphery
5   thereof of the mat 16. Description is given below on
the mosaic segment redundancy, with reference to Fig.
5. It should be noted that a portion shown in Fig. 5
corresponds to a portion shown in Fig. 2 in which the
conventional technique is described, each having the
10 same memory size.

The mat 16 further has a sub mat decoder 31,
a redundancy sub mat decoder 32, and an OR circuit 33
as common circuits of each sub mat in addition to the
column address decoder 18 and the I/O circuit 19.
15 The mat 16 further has the eight sub mats 17-0 to 17-
7.

The sub mat decoder 31 is a decoder for
selecting the sub mats 17-0 to 17-7 based on the
upper bits of the row address. The sub mat decoder
20 31 receives and decodes the row address X11 to X13,
and outputs sub mat selection signals SM0 to SM7.
The sub mat selection signals SM0 to SM7 are supplied
to respective of the sub mats 17-0 to 17-7, and the
corresponding sub mat 17 is activated.
25   The redundancy sub mat decoder 32 selects
redundancy ROM circuits 28 in the sub mat 17 based on
the lower bits of the row address. Supplied to the

26

redundancy sub mat decoder 32 are the row address X0

to X2 and an access activation signal AE which is

activated when the mat 16 is to be activated.

Redundancy activation signals BE0 to BE7 obtained by

5 decoding the row address X0 to X2 are outputted to

the redundancy ROM circuits 28 of the sub mats 17-0

to 17-7, respectively. In this manner, the

redundancy ROM circuits 28 are activated by the

redundancy activation signal BE independently of the

10 sub mat selection signal SM.

The OR circuit 33 collects from the sub mats

17-0 to 17-7 eight redundancy selection signals RE-n-

0 to RE-n-7 outputted from respective of the

redundancy ROM circuits 28 in the sub mat 17. The

15 logical sum of the collected 64 redundancy selection

signals RE is outputted as a row address decoder

killer signal XDK. The row address decoder killer

signal XDK is supplied to the sub mats 17-0 to 17-7

to inactivate the row address decoders 22-0 to 22-7.

20 In this case, the memory cell arrays 21-0 to 21-7 are

not activated.

The column address decoder 18 selects one of

the sense amplifiers 25-0 to 25-7 based on the column

address (Y address), and activates the selected one.

25 The sub mat 17-0 is provided with the memory

cell array 21-0, the row address decoder 22-0, the

redundancy memory cell array 23-0, the redundancy row

address decoder 24-0, a sub word decoder 27-0, the redundancy ROM circuits 28-0-0 to 28-0-7, and the sense amplifier 25-0. The other sub mats 17-1 to 17-7 have the same configurations as the sub mat 17-0, and the sub mat selection signal SM and the redundancy activation signal BE are supplied to each of the sub mats. For this reason, description is given below on the sub mat 17-0, and is omitted on the other sub mats 17-1 to 17-7.

In the memory cell array 21-0, the memory cells are arranged in a matrix form. The memory cells are selected by the row address decoder 22-0, the sub word decoder 27-0, and the column address decoder 18. The memory cell array 21-0 has 2048 word lines in a row direction. One word line is selected by outputs of the row address decoder 22-0 and the sub word decoder 27-0, and a sub memory block 35n which is a memory cell group (row) connected to the selected word line is activated. In the present embodiment, the sub memory block 25n is a segment 20 which is a unit replaced when a defect occurs in the memory cell.

The row address decoder 22-0 decodes the row address (X address) of the memory cell array 21-0. The row address to be decoded is the row address X3 to X10 among the row address X0 to X10 in which the upper three bits for selecting the sub mat 17-0 are

excluded. The lower three bits X0 to X2 of the row
address are decoded by the sub word decoder 27-0.
The input row address X3 to 10 is decoded, and one of
the 256 main word lines MWD is activated.

5   The redundancy memory cell array 23-0 is a
redundancy memory block for replacing the data when
the memory cell array has a defect. The redundancy
memory cell array 23-0 has eight word lines and eight
redundancy sub memory blocks 35r connected to

10 respective of the word lines. In the present
embodiment, the unit for the replacement of the
defective portion is a sub memory block corresponding
to one word line, and so eight redundancy segments 26
are provided. The redundancy selection signals RE-0-

15 0 to RE-0-7 are decoded by the redundancy row address
decoder 24-0, and a redundancy main word line RMWD of
the redundancy memory cell array 23-0 is activated.
When the redundancy main word line RMWD is activated,
one of the redundancy sub memory blocks 35r-0 to 35r-

20 7 is selected. The selected redundancy sub memory
block substitutes for one of the sub memory blocks
35n having a defect generated in the memory cell
array 21. That is to say, the segment 20 having the
defect is replaced by the redundancy segment 26.

25   The redundancy row address decoder 24-0
receives the redundancy selection signals RE-0-0 to
RE-0-7 outputted from the redundancy ROM circuits 28-

0-0 to 28-0-7, and activates the redundancy main word
line RMWD of the corresponding redundancy memory cell
array 23-0. In the case of Fig. 5, the redundancy
memory cell array 23-0 has eight redundancy main word

5   lines RMWD corresponding to respective of the
redundancy ROM circuits 28-0-0 to 28-0-7. When any
of the redundancy selection signals RE-0-0 to RE-0-7
is activated, the redundancy row address decoder 24-0
activates one corresponding redundancy main word line

10   RMWD.

          The sub word decoder 27-0 decodes the lower
three bits X0 to X2 of the row address to select one
sub word line SWD and activate the selected sub
memory block 35n. The sub word line SWD is driven by

15   a sub word driver 29 receiving a signal decoded by
the sub word decoder 27-0 and the main word line MWD,
and selects the sub memory block. As compared with
the sub word decoder 89 of the conventional technique
shown in Fig. 2, the sub word decoder 27 of the

20   present invention has a simplified configuration,
since a selector for switching a signal that selects
the sub word line SWD is unnecessary and the
redundancy selection signal RE is not input.
Consequently, it is also possible to reduce the delay

25   time due to the signal switching and to increase the
operation speed. Alternatively, the sub word decoder
27-0 may have the same configuration as the

conventional technique shown in Fig. 2. In this case,
the number of the redundancy main word line is one,
and the main word line and the sub word line of the
redundancy memory cell array 23-0 are switched by the
5   selector.

The redundancy ROM circuits 28-0-0 to 28-0-7
hold defective addresses for specifying the defective
memory cells of the memory cell arrays 21-0 to 21-7
in the mat 16, and determines whether or not to
10 select the redundancy memory cell array 23-0. The
redundancy selection signals RE-0-0 to RE-0-7 are
activated when the redundancy memory cell array 23-0
is selected. The defective addresses of the memory
cell arrays 21-0 to 21-7 correspond to the row
15 address X3 to X13 including the address for selecting
the sub mat, and are programmed into the fuses
provided in the redundancy ROM circuits 28-0-0 to 28-
0-7. At the time of an initial operation, the
defective address held in the fuses is latched by a
20 latch circuit. In normal read/write operations, when
the redundancy activation signal BE0 is inputted, the
input row address X3 to X13 and the defective address
held in the latch circuit are compared in an .address
comparator. In a case of match as a result of the
25 comparison, the input row address X3 to X13 is
regarded as the defective address, and the redundancy
selection signal RE is activated. In a case of

mismatch, the redundancy selection signal RE is not
activated. Eight redundancy ROM circuits 28 are
provided to the sub mat 17-0, and hold a maximum of
eight defective addresses for specifying the
5   defective memory cells.

The sense amplifier 25-0 is a sense amplifier
for reading data from the memory cells of the memory
cell array 21-0 and the redundancy memory cell array
23-0. The sense amplifier is selected by the column
10 address decoder 18. The output of the selected sense
amplifier 25 is outputted as data stored in the
memory.

As described above, when the row address is
supplied to the sub mat decoder 31, the row address
15 decoder 22, the sub word decoder 27 and the
redundancy sub mat decoder 32, the allocation
relationship between the memory cell array 21 and the
redundancy memory cell array 23 is determined. The
redundancy memory cell arrays 23-0 to 23-7 are
20 provided for the memory cell arrays 21-0 to 21-7 in
the eight sub mats 17-0 to 17-7, respectively. Each
of the memory cell arrays 21 has a configuration in
which an array of eight sub word lines selected by
the sub word decoder 27 receiving the row address X0
25 to X2 is repeated for 256 times. The 256 arrays of
the eight sub word lines are selected by the row
address decoder 22 for decoding the row address X3 to

32

X10.

On the other hand, the redundancy sub mat decoder 32 selects the sub mat based on the row address X0 to X2. The redundancy memory cell array used for the replacement is arranged in the selected sub mat. Therefore, the array of the eight sub word lines and eight sub mats are related to each other with the same row address X0 to X2. That is, respective of the sub memory blocks 35n connected to the eight sub word lines are allocated sequentially to eight redundancy memory cell arrays. Furthermore, since the array of the eight sub word lines is repeated by the row address X3 to X10, the array is also allocated cyclically and sequentially to the redundancy memory cell arrays.

In addition, the same redundancy memory cell array 23-m (m=0 to 7) is recurrently allocated to every eight sub memory block 35-n (n= 0 to 2047). In other words, the sub memory block 35n-n that satisfies the condition of n=8×A+m, is allocated to the redundancy memory cell array 23-m (m= 0 to 7). Here, the A is a value determined by the row address X3 to X10, and is an address indicative of the main word line according to the present embodiment. That is to say, the sub memory blocks 35n allocated to a redundancy memory cell array 23-x (redundancy memory block) all has the same sub word line number

indicated by the row address X0 to X2.

Next, the redundancy ROM circuit is explained.
Fig. 6 is a block diagram showing a configuration of
the redundancy ROM circuits 28-0-0 to 28-0-7 provided
5   in the sub mat 17-0. Since the redundancy ROM
circuits 28-0-0 to 28-0-7 have the same configuration,
description is given below by using the reference
numeral 28. The redundancy ROM circuit 28 has
redundancy fuse circuits 41-3 to 41-13, a NOR circuit
10   50 constituted by N-type MOS transistors 49-3 to 49-
13, a P-type MOS transistor 46, an N-type MOS
transistor 48, inverter circuits 51 and 52, and a P-
type MOS transistor 53.

Each of the redundancy fuse circuits 41-3 to
15   41-13 has a fuse 44, a P-type MOS transistor 45, a
latch circuit 42, and an exclusive OR circuit 43.
The fuse 44 holds information of one bit of the
defective address specifying the defective memory
cell. The P-type MOS transistor 45 precharges the
20   fuse 44 in response to a reset signal RST. The latch
circuit 42 holds a result of precharging the fuse 44.
The information of one bit of the defective address
held by the latch circuit 42 and one bit of the input
address signal X3 to X13 are compared with each other
25   by the exclusive OR circuit 43. In a case of
mismatch, the exclusive OR circuit 43 activates the
output to the NOR circuit 50.

The P-type MOS transistor 46 and the N-type
MOS transistor 48 drives the NOR circuit 50 in
response to the redundancy activation signal BE for
activating the address comparison. When the
5   redundancy activation signal BE is in an inactive
state, the P-type MOS transistor 46 is turned on and
precharges the NOR circuit 50. When the redundancy
activation signal BE is activated, the N-type MOS
transistor 48 is turned on, sources of the N-type MOS
10 transistors 49-3 to 49-13 are grounded, and the
output to the inverter circuit 51 is determined by
the result of the address comparison outputted from
the redundancy fuse circuits 41-3 to 41-13. When
address mismatch is detected in any of the redundancy
15 fuse circuits 41-3 to 41-13, the output of the
redundancy fuse circuit 41 activates the N-type MOS
transistor 49, and discharges a precharged potential.
Therefore, only when the compared addresses are all
matched and the outputs from the redundancy fuse
20 circuits 41 are all inactivated, the input of the
inverter circuit 51 is activated, which indicates
that the addresses are matched.

The inverter circuits 51 and 52 and the P-
type MOS transistor 53 form a latch circuit and hold
25 the output of the NOR circuit 50. The output of the
inverter circuit 52 is outputted from the redundancy
ROM circuit 28 as the redundancy selection signal RE

for selecting the redundancy memory at the time of activation.

In such a configuration, one redundancy ROM circuit 28 has eleven fuses 44 in correspondence to the row address X3 to X13.

Next, the main word line and the sub word line are described. Fig. 7A is a figure for explaining a relationship between the main word line MWD and the sub word line SWD in the memory cell array 21. The row address X3 to X10 is decoded by the row address decoder 22, and one of the main word lines MWD is activated. Since the row address to be inputted has eight bits, one of 256 main word lines MWD is activated.

The row address X0 to X2 is decoded by the sub word decoder 27, and one of eight lower row address decode signals is activated. As shown in Fig. 7A, the sub word drivers 29-0 to 29-7 are arranged at respective of intersections between eight lower row address decode signal lines and main word lines MWD.

The sub word driver 29 inputs intersecting main word line MWD and the lower row address decode signal, and activates the sub word line SWD. The sub word driver 29 functions as a switch constituted by a P-type MOS transistor and an N-type MOS transistor. When the main word line MWD is activated, the P-type MOS transistor is turned on, and a status of the

lower row address decode signal is reflected to the sub word line SWD. When the main word line MWD is inactive, the N-type MOS transistor is turned on, and the sub word line SWD gets into the inactive state.

5 Therefore, the sub word line SWD is activated when both the main word line MWD and the lower row address decode signal are in the active state. Thus, one sub word line SWD is selected by the row address X0 to X10.

10 When the sub word line SWD is activated, memory cells connected to the sub word line SWD is activated. For example, when the sub word line SWD outputted from the sub word driver 29-7 is activated, a sub memory block which is a memory cell group

15 connected to the sub word line SWD is activated. In the present embodiment, the sub memory block is the segment as the unit for the replacement of the memory cell having a defect, and the segment 20-7 is activated. The sub memory blocks 35-0 to 35-7 have

20 memory cells as indicated by the reference numeral 30 at every intersections between the sub word lines SWD and the bit lines. The status of the memory cell to be activated appears in the bit line intersecting with the sub word line SWD. Data stored in the

25 activated memory cell is read by the sense amplifier 25 selected by the column address decoder 18. Also, data inputted from the outside is written into the

activated memory cell.

In the redundancy memory cell array 23, a relationship between the redundancy main word line RMWD and the redundancy sub word line RSWD is similar to the relationship between the main word line MWD and the sub word line SWD in the memory cell array 21. Fig. 7B shows a relationship in the sub mat 17-0. In the redundancy row address decoder 24, address information to be inputted is not the row address but the redundancy selection signals RE-0-0 to RE-0-7 outputted from the redundancy ROM circuits 28-0-0 to 28-0-7. Also, in the present embodiment, the number of the redundancy main word lines RMWD is eight in correspondence to the redundancy selection signals RE-0-0 to RE-0-7. Each of the redundancy main word lines RMWD corresponds to one redundancy sub word line RSWD.

The redundancy row address decoder 24-0 receives the redundancy selection signals RE-0-0 to RE-0-7, and activates the redundancy main word line RMWD that corresponds to the redundancy selection signals RE-0-0 to RE-0-7. On the other hand, the sub word decoder 27-0 receives the row address X0 to X2, and outputs eight decode signals. All the sub word driver 29-0 to 29-7 are connected to a decode signal "0" corresponding to all the row address X0 to X2 being "0" among the eight decode signals. Thus, in

the sub mat 17-0, the sub word driver 29 is connected

to a signal corresponding to the row address X0 to X2

being "0", while in the sub mat 17-n, the sub word

driver 29 is connected to a decode signal

5 corresponding to the row address X0 to X2 being "n".

According to the sub word driver 29 thus connected,

when the redundancy main word line RMWD is activated

in the sub mat 17-0, the redundancy sub word line

RSWD is activated only when the lower three bits X0

10 to X2 of the row address are "0". The status of the

memory cell of the redundancy memory cell array 23

appears at the bit line intersecting with the

redundancy sub word line RSWD. Since the activation

of the memory cell array 21 is prohibited by the row

15 address decoder killer signal XDK, data stored in the

redundancy memory cell is read by the sense amplifier

25 selected by the column address decoder 18, and

data inputted from the outside is written. In the

sub mat 17-1 to 17-7 as well, the redundancy sub word

20 line RSWD is activated and a defect is repaired when

the lower three bits (X0 to X2) of the row addresses

indicate respective of "1" to "7" and the redundancy

selection signal RE is activated.

Fig. 8 shows a time chart describing an

25 operation. The reset signal RST as shown in (a)

section of Fig. 8 is inputted from the control

circuit 11 after the power-on. When the reset signal

RST is inputted, the P-type MOS transistor 45 shown in Fig. 6 is activated, and a voltage is applied to the fuse 44 that holds the defective address identifying the defective memory cell. A voltage

5 level inputted to the latch circuit 42 varies based on blowing/not-blowing of the fuse 44. The latch circuit 42 holds the state of the fuse.

The voltage level that corresponds to the blowing/not-blowing differs depending on the type of

10 fuse element. In a case of a melting type, the voltage level becomes high in the case of blowing, while becomes low in the case of not-blowing. Also, in a case of a type in which an insulating film is destroyed, the voltage level becomes low in the case

15 of blowing (destruction), while becomes low in the case of not-blowing (non-destruction). The voltage level applied to the fuse 44 is held by the latch circuit 42, and the address held in the latch circuit 42 is used for the address comparison at the time of

20 normal memory read/write memory access.

As shown in the first half of Fig. 8, when both the redundancy activation signal BE ((b) section) and the row address Xn ((c) section: X3 to X13) are inputted to the redundancy ROM circuit, the

25 address comparison is carried out.

If the access address does not match defective address specifying the defective memory

cell, the redundancy selection signal RE ((d) section) is not activated. If all the redundancy selection signals RE are not activated, the row address decoder killer signal XDK is not activated.

5 The row address decoder 22-0 becomes effective, the main word line MWD is activated ((e) section: Low level), and thereby the corresponding sub word line SWD is activated ((f) section: High level). Also, the redundancy main word line RMWD for accessing the

10 redundancy memory cell array is inactive ((g) section: High level), and the corresponding redundancy sub word line RSWD is also inactive ((h) section: Low level). In this case therefore, the memory cell in the memory cell array 21-0 is accessed.

15 As shown in the second half of Fig. 8, both the redundancy activation signal BE ((b) section) and the row address Xn ((c) section: X3 to X13) are inputted to the redundancy ROM circuit. When the row address Xn matches the defective address specifying

20 the defective memory cell, the redundancy selection signal RE ((d) section) is activated. When the redundancy selection signal RE is activated, the row address decoder killer signal XDK is generated in the OR circuit 33, and the row address decoder 22-0 is

25 inactivated. Thus, the main word line MWD is inactivated ((e) section: High level), and the sub word line SWD remains inactive ((f) section: Low

level) even if the output of the sub word decoder 27-0 is activated. The redundancy main word line RMWD ((g) section) of the redundancy memory cell array 23-0 is activated because the redundancy selection

5 signal RE is activated. The redundancy sub word line RSWD that corresponds to the output of the sub word decoder 27-0 is activated ((h) section: High level), and the corresponding memory cell in the redundancy memory cell array 23-0 is accessed.

10   Description is given on the allocation relationship between the memory cell and the redundancy memory cell array when a defect occurs. According to the mosaic segment redundancy, when a defective memory cell group 55 is generated in the

15 memory cell array 21-0 as shown in Fig. 9, the redundancy memory cell arrays 23-0 to 23-2 are allocated in accordance with the defective memory cell group 55. In the redundancy memory cell arrays, respective portions indicated by the reference

20 numerals 56-0 to 56-2 correspond to the defective memory cell group 55. According to the conventional technique shown in Fig. 1B, the defect generated in the three segments are repaired by using the three segments in the redundancy memory block 74. When the

25 present invention is applied, as shown in Fig. 9, the repair is possible by using the redundancy memory cell arrays 23-0-0, 23-1-0 and 23-2-0 which are the

redundancy segments in respective of the redundancy memory cell arrays 23-0 to 23-2 as the redundancy memory blocks.

Shown in Fig. 9 is the replacement of the defect generated in the memory cell group connected to the three successive sub word lines, namely, the three sub memory blocks. Description is given on a case where a defect is generated over further successive sub word lines, e.g. where a memory cell group is defective, the memory cell group being connected to twelve successive sub word lines of the successive sub word lines 0 to 7 corresponding to one main word line and the sub word lines 0 to 3 corresponding to the next main word line in the memory cell array 21-0. According to the conventional method in which the memory cell array 21-0 is related to the redundancy memory cell array 23-0, the repair is impossible because the number of the redundancies in the redundancy cell array 23-0, which is eight, is insufficient. According to the present invention, a defect generated in the memory cell array 21-0 is repaired by the redundancy memory cell arrays 23-0 to 23-7. The segments having the defect in the memory cell array 21-0 are sequentially allocated to the redundancy memory cell arrays 23-0 to 23-7. Two redundancy word lines are used in each of the redundancy memory cell arrays 23-0 to 23-3,

and one redundancy word line is used in each of the
redundancy memory cell arrays 23-4 to 23-7. Thus,
the repair is possible. Therefore, a redundancy
memory having high repair efficiency can be

5   configured with the same number of redundancy
memories and fuses as that of the redundancy circuit
of the conventional technique.

         According to the mosaic segment redundancy,
the number of fuses in the redundancy circuit holding

10 the defective address specifying the defective memory
cell is eleven corresponding to the row address X3 to
X13, and the repair of the defective memory cell is
possible by using these fuses. In order to repair
the same defect by using the flexible method of the

15 conventional technique, fourteen fuses that
correspond to the row address X0 to X13 are necessary
as the fuses for holding the defective address, since
it is judged whether or not the access row address
matches the defective address specifying the

20 defective memory cell. As described above, a
concentrated defect repaired by using fourteen fuses
in the conventional flexible method can be repaired
by using eleven fuses when the present invention is
applied. Thus, the number of fuses can be reduced.

25   The present embodiment has been described by
using the memory cell group connected to one word
line as the segment; however, there is no limitation

to the one word line. If a range can be specified by one address and it is a unit which can be replaced by the redundancy memory, the range may be used as the segment. Also, the redundancy for the word line (row

5 address) has been described. It is obvious that the present invention can be applied to redundancy for the bit line (column address) as well.

Referring next to Fig. 10, description is given on a semiconductor memory device according to

10 the second embodiment of the present invention. In the second embodiment, the defect of a memory cell group corresponding to a plurality of sub words is repaired as a segment which is a repair unit. As compared with the first embodiment, the number of

15 fuses used for holding a defective address specifying a defective memory cell can be further reduced. Fig. 10 shows a case where a memory cell group associated with two sub words is a segment and a defect is replaced. The same applies to a unit of more than

20 two sub words. As compared with the case in the first embodiment, the number of fuses holding the defective address specifying the defective memory cell is reduced by half, since the defect is replaced in units of two sub words. Here, description is

25 given on an allocation relationship between a memory cell array 21a and a redundancy memory cell array 23a in a row address. Therefore, only a portion that is

relevant to the row address, the address decoder and the memory cell array is shown, and the other portions are omitted. Additionally, the redundancy for the word line (row address) is described below,

5 which is obviously applicable to the redundancy for the bit line (column address) as well.

A DRAM has a sub mat decoder 31a, memory cell arrays 21a-0 to 21a-7, row address decoders 22a-0 to 22a-7, redundancy memory cell arrays 23a-0 to 23a-7,

10 redundancy row address decoders 24a-0 to 24a-7, redundancy ROM circuit groups 28a-0 to 28a-7 each having four redundancy ROM circuits, and a redundancy sub mat decoder 32a. A sub word decoder not shown receives the row address X0 to X2. A method of

15 selecting words in the memory cell array is the same as in the first embodiment, and word selecting in the redundancy memory cell array is described with reference to Fig. 7C.

The sub mat decoder 31a receives the row

20 address X11 to X13, and outputs the sub mat selection signals SM0 to SM7 to respective sub mats. The row address decoders 22a-0 to 22a-7 of each of the sub mats receive the row address X3 to X10, the sub word decoder receives the row address X0 to X2, and one of

25 2048 word lines of each of the memory cell arrays 21a-0 to 21a-7 is activated. The memory cell arrays 21a-0 to 21a-7 of each of the sub mats are activated

by the corresponding sub mat selection signals SM0 to SM7 from the sub mat decoder 31a, and output data of the memory cell that corresponds to the row address decoders 22a-0 to 22a-7 and the activated word line.

5 The redundancy sub mat decoder 32a receives the row address X1 and X2, and outputs four redundancy activation signals BE0 to BE3. The four redundancy activation signals BE0 to BE3 are supplied to the redundancy ROM circuit groups 28a-0 and 28a-1, 28a-2

10 and 28a-3, 28a-4 and 28a-5, and 28a-6 and 28a-7, respectively. Therefore, two redundancy ROM circuit groups are activated by one redundancy activation signal BE. The redundancy ROM circuit group 28a-n (n= 0 to 7) receives the row address X3 to X13, and

15 outputs a comparison result with the defective address specifying the defective memory cell, as the redundancy selection signals RE-n-0 to RE-n-3, to the redundancy row address decoder 24a-n. The redundancy row address decoder 24a-n receives the redundancy

20 selection signals RE-n-0 to RE-n-3, and activates the redundancy main word line RMWD of the redundancy memory cell array 23a-n (n= 0 to 7). A redundancy ROM circuit provided to the redundancy ROM circuit group 28a-n is related to two sub word lines of the

25 redundancy memory cell arrays 23a-0 to 23a-7. Therefore, two sub word drivers 29 are connected to one redundancy main word line RMWD. The redundancy

memory cell arrays 23a-0 to 23a-7 each have four main word lines driven by the redundancy row address decoders 24-0 to 24-7, and output the data of the memory cell connected to the sub word line activated

5 by the sub word driver 29.

Each of the memory cell arrays 21a-0 to 21a-7 has 2048 word lines, and one word line is selected by the row address decoders 22a-0 to 22a-7 receiving and decoding the row address X0 to X10 and the sub word

10 decoder. When all the redundancy ROM circuits 28a determine that the accessed address does not match the defective address, a relevant memory cell row among the memory cell arrays 21a-0 to 21a-7 is accessed. When any of the redundancy ROM circuits

15 28a determines that the accessed address matches the defective address, the row address decoder killer signal is activated, and the row address decoders 22a-0 to 22a-7 are invalidated. Therefore, the memory cells of the memory cell arrays 21a-0 to 21a-7

20 are not accessed.

The redundancy sub mat decoder 32a decodes the row address X1 and X2, and outputs four redundancy activation signals BE0 to BE3. One redundancy activation signal BE selects two

25 redundancy ROM circuit groups (28a-0 and 28a-1, or 28a-2 and 28a-3, or 28a-4 and 28a-5, or 28a-6 and 28a-7). Therefore, each of the redundancy ROM

circuit groups 28a-0 and 28a-1, 28a-2 and 28a-3, 28a-4 and 28a-5, and 28a-6 and 28a-7, can be regarded as one redundancy ROM circuit group and can be considered as a memory having four redundancy memories.

The redundancy memory cell arrays 23a-0 to 23a-7, each having eight word lines, are redundancy memory blocks for replacing the data at the defective address specifying the defective memory cell in the memory cell arrays 21a-0 to 21a-7. Eight word lines of the redundancy memory cell array 23a-n corresponds in pairs to respective of the redundancy selection signals RE-n-0 to RE-n-3 outputted from the redundancy ROM circuit group 28a-n (n= 0 to 7). The redundancy selection signals RE-n-0 to RE-n-3 each activates one redundancy main word line RMWD by the redundancy row address decoder 24a-n (n= 0 to 7). One redundancy main word line is connected to two sub word drivers 29, and one redundancy sub word line RSWD is selected by the row address X0. The row address X0 is not inputted to the redundancy sub mat decoder 32a, and one of the redundancy ROM circuits activated by the outputted redundancy activation signal BE is related to two word lines. Therefore, the two word lines correspond to two adjacent word lines in the memory cell arrays 21a-0 to 21a-7.

Here, description is given on a relationship

between the main word lines and the sub word lines in

the redundancy memory cell arrays 23a-0 to 23a-7, and

on an allocation relationship between the sub memory

block having a defect in the memory cell arrays 21a-0

5   to 21a-7 and the redundancy sub memory block in the

redundancy memory cell arrays 23a-0 to 23a-7 for

replacing the sub memory block. The relationship

between the main word lines and the sub word lines in

the memory cell arrays 21a-0 to 21a-7 was described

10   in the first embodiment by referring to Fig. 7A.

Since the same applies to the present embodiment,

description is omitted. Description is made on the

relationship between the main word lines and the sub

word lines in the redundancy memory cell arrays 23a-0

15   to 23a-7 with reference to Fig. 7C. Fig. 7 shows the

redundancy memory cell array 23a-0 in the sub mat 17-

0, and relevant redundancy row address decoder 24a-0,

sub word decoder 27a-0, sense amplifier 25-0, and

column address decoder 18.

20   The redundancy row address decoder 24a-0

receives the redundancy selection signals RE-0-0 to

RE-0-3, and activates one redundancy main word line

RMWD that corresponds to the activated redundancy

selection signal RE among four redundancy main word

25   lines RMWD corresponding to the redundancy selection

signals RE-0-0 to RE-0-3. The sub word decoder 27a-0

outputs eight decode signals activated in accordance

with the row address X0 to X2. In the redundancy

memory array 23a-0, the sub word driver 29 activates

the redundancy sub word line RSWD based on the

activated decode signal and the redundancy main word

5 line RMWD, and a sub memory block 35 which is the

memory cell group connected to the redundancy sub

word line RSWD is activated. The sense amplifier 25-

0 is selected by the column address decoder 18 based

on the column address. Data stored in the activated

10 memory cell is read by the sense amplifier 25-0, and

data inputted from the outside is written thereto.

The sub word decoder 27a-0 outputs eight

decode signals activated based on the row address X0

to X2. The sub word drivers 29-0 to 29-7 are

15 arranged at intersections between the decode signal

lines and the redundancy main word lines. The sub

word drivers 29-0 to 29-7 each activates one

redundancy sub word line RSWD, based on the

redundancy main word line RMWD and the decode signal.

20 Fig. 7C shows the redundancy memory cell array 23a-0

arranged in the sub mat 17-0, where the sub word

drivers 29-0, 2, 4, and 6 receive decode signals

activated when the row address X0 to X2 is "0", and

the sub word drivers 29-1, 3, 5, and 7 receive decode

25 signals activated when the row address X0 to X2 is

"1". Such connection makes it possible to specify a

sub memory block in the segment. In the case of

other sub mats, the sub word drivers 29-0, 2, 4, and

6 receive decode signals activated when the row

address X0 to X2 is "2×n", and the sub word drivers

29-1, 3, 5, and 7 receive decode signals activated

5 when the row address X0 to X2 is "2×n+1" (n= 0, 1, 2,

and 3), in the redundancy memory cell array 23-(2×n)

and the redundancy memory cell array 23-(2×n+1).

The segment in such a configuration

corresponds to two sub memory blocks, the segment

10 being an allocation unit for repairing the defect of

the memory cell array by using the redundancy memory

array. Therefore, the sub memory blocks 35-0 and 35-

1 are allocated as a redundancy segment 26-0; the sub

memory blocks 35-2 and 35-3 are allocated as a

15 redundancy segment 26-1; the sub memory blocks 35-4

and 35-5 are allocated as a redundancy segment 26-2;

and the sub memory blocks 35-6 and 35-7 are allocated

as a redundancy segment 26-3, wherein the allocated

redundancy segment substitutes for the defect

20 generated in two adjacent sub words of the memory

arrays 21-0 to 21-7. The allocated redundancy

segment repairs the defect by substituting for one

sub memory block of the memory cell arrays 21a-0 to

21a-7 having the defect and being accessed.

25 An operation when the memory is accessed is

described. When the memory is accessed, the

redundancy ROM circuit groups 28a-0 to 28a-7 are

activated in combinations of 28a-0 and 28a-1, 28a-2

and 28a-3, 28a-4 and 28a-5, and 28a-6 and 28a-7

simultaneously. Each of the redundancy ROM circuit

groups 28a-0 to 28a-7 has four redundancy ROM

5 circuits 28a-n-0 to 28a-n-3 (n= 0 to 7), and compares

the defective address specifying the defective memory

cell held in the fuses of each circuit and the input

row address X3 to X13. In the case of match, the row

address X3 to X13 is determined to be the defective

10 address, and one redundancy selection signal RE is

activated. The redundancy main word line and the sub

word line are selected, the redundancy main word line

corresponding to the activated redundancy selection

signal RE-n-m outputted from the redundancy ROM

15 circuit 28a-n-m (n= 0 to 7, m= 0 to 3) holding the

defective address. Then, the redundancy memory cell

array 23a-n is activated, and all the memory cell

arrays 21a-0 to 21a-7 are inactivated. Therefore,

the redundancy memory cell array 23a is accessed

20 instead of the memory cell array 21a, and the defect

of the memory cell array 21a is replaced by the

redundancy memory cell array 23a. In the case of

mismatch, the accessed address is regarded not to be

the defective address specifying the defective memory

25 cell, and the memory cell array 21a is activated and

normal access is performed.

Each of the redundancy ROM circuits 28a-0 to

28a-7, when activated by the redundancy activation
signals BE0 to BE 3, compares the defective address
specifying the defective memory cell held in the fuse
and the input row address X3 to X13. Therefore, the

5   row address X1 to X13 is compared with the defective
address, and the memory cells that belong to two
adjacent sub words corresponding to the row address
X0 are the target of replacement (segment).

Thus, the segment which is the allocation

10 unit for replacing the defect is two sub memory
blocks. In the memory cell array 21a-0 selected by
the row address X0 to X10, the memory cell arrays
21a-0-0 and 21a-0-1 are allocated to the redundancy
memory cell array 23a-0 or 23a-1, the memory cell

15 arrays 21a-0-2 and 21a-0-3 are allocated to the
redundancy memory cell array 23a-2 or 23a-3, the
memory cell arrays 21a-0-4 and 21a-0-5 are allocated
to the redundancy memory cell array 23a-4 or 23a-5,
the memory cell arrays 21a-0-6 and 21a-0-7 are

20 allocated to the redundancy memory cell array 23a-6
or 23a-7, and the memory cell arrays 21a-0-8 and 21a-
0-9 are allocated to the redundancy memory cell array
23a-0 or 23a-1. Thus, the segments are cyclically
allocated in order. In other words, the memory cell

25 arrays 21a-0-0 to 21a-0-2047 are repeatedly allocated
in units of two sub memory blocks, to the pairs of
the sub memory blocks (23a-0 and 23a-1, 23a-2 and

23a-3, 23a-4 and 23a-5, and 23a-6 and 23a-7) of the
redundancy memory cell arrays, in accordance with the
row address X1 and X2.

Further, in the memory cell arrays 21a-1 to
5 21a-7, as in the case of the memory cell array 21a-0,
the memory cell arrays 21a-i-(2×m) and 21a-i-(2×m+1)
are allocated sequentially to the redundancy memory
cell array 23a-(2×n) or 23a-(2×n+1) (i= 1 to 7, m= 0
to 1023, n= 0 to 3, m is the number of segments
10 provided to the memory cell array, n is given by a
reminder generated when m is divided by 4 as the
number of the redundancy memory blocks).

In other words, the following description is
.possible. The redundancy memory cell arrays 23a-0 to
15 23a-7 are provided in correspondence to the memory
cell arrays 21a-0 to 21a-7. Each of the memory cell
arrays 21a has 1024 segments, wherein memory array
groups connected to two adjacent sub word lines
selected by the row address X0 is the segment being a
20 unit replaced when the defective memory cell is
generated. Based on the row address X1 and X2, the
memory cell array 21a can be considered as segment
groups whose unit is four adjacent segments from
which one segment can be selected. In the viewpoint,
25 the memory cell array 21a has 256 segment groups
which are arranged repeatedly and are selected based
on the row address X3 to X10. On the other hand, a

sub mat in which the redundancy memory cell array is arranged is selected by the redundancy sub mat decoder 32a to which the row address X1 and X2 are inputted. At this time, the output of the redundancy

5   sub mat decoder 32a is inputted as the same signal to every two circuit groups of the redundancy ROM circuit groups 28a. That is, each of the redundancy ROM circuit groups 28a-0 and 28a-1, 28a-2 and 28a-3, 28a-4 and 28a-5, and 28a-6 and 28a-7 can be

10 considered as one redundancy ROM circuit group. In that case, the number of the redundancy circuit groups is four. Therefore, four segments forming the segment group and four redundancy ROM circuit groups are selected by the same row address X1 and X2,

15 having the corresponding relationship. In other words, the four segments are sequentially allocated to the redundancy memory cell arrays connected to the four redundancy ROM circuit groups. Further, since the four segments are repeated due to the row address

20 X3 to X10, the four segments are cyclically allocated in order to the redundancy memory cell arrays as well.

Also, the segment n (n= 0 to 1023) is recurrently allocated in units of four to the same redundancy memory cell array group m (combination of

25 the redundancy memory cell array 23-(2×m) and the redundancy memory cell array 23-(2×m+1)) (m= 0 to 3). Therefore, the segment n that satisfies the

relationship of n= 4×A+m is allocated to the redundancy memory cell array group m (m= 0 to 3). Here, A is a value determined by the row address X3 to X10. That is to say, the segment x allocated to

5 the redundancy memory cell array group x all has the same segment number that is specified by the row address X1 and X2.

By performing such allocation to the redundancy memory cell array, one redundancy ROM

10 circuit 28a corresponds to two sub word lines. As compared with the case where redundancy memory cell arrays having the same capacity is used, the number of circuits is reduced by half. In the case of Fig. 10, the number of circuits is four. Therefore, the

15 defect can be repaired under the state where the fuses for holding the defective address specifying the defective memory cell are also reduced by half.

Additionally, the redundancy for the word line (row address) has been described in the present

20 embodiment, which is obviously applicable to the redundancy for the bit line (column address) as well.

In addition, a combination of the first embodiment and the second embodiment is also effective. Half of the redundancy circuits in each

25 sub mat are configured to conduct the repair in units of one sub word as in the case of the first embodiment, and the other half are configured to

conduct the repair in units of two sub words as in the case of the second embodiment. Alternatively, the redundancy circuits of half of the sub mats are configured to conduct the repair in units of one sub

5   word as in the case of the first embodiment, and the redundancy circuits of the other half of the sub mats are configured to conduct the repair in units of two sub words as in the case of the second embodiment. By adopting such a combined configuration, it is

10   possible to realize more detailed treatment depending on the status of the defects, which is effective for reduction in the number of the redundancy circuits, particularly that of the fuses.

A third embodiment is described with

15   reference to Fig. 11. In the third embodiment, the defect is repaired with the use of a redundancy circuit, using a memory cell group corresponding to a plurality of sub words as a segment which is a defect repair unit. As compared with the second embodiment,

20   a bit length holding the defective address specifying the defect location is reduced, and the number of fuses used is reduced. In other words, the fuse corresponding to the row address X3 holding a defective address is eliminated, inputted to the

25   redundancy sub mat decoder. Consequently, one memory array and one redundancy array in a sub mat are related one-to-one. Fig. 11 shows a case where

replacement is performed in units of two sub words as the segment. Since an allocation relationship between a memory cell array 21b and a redundancy memory cell array 23b in the row address is described

5 here, only a portion relevant to the row address, the address decoder and the memory cell array is shown, and other portions are omitted. Additionally, description is given below on redundancy for a word line (row address), which is obviously applicable to

10 redundancy for a bit line (column address) as well.

A DRAM has a sub mat decoder 31b, memory cell arrays 21b-0 to 21b-7, row address decoders 22b-0 to 22b-7, redundancy memory cell arrays 23b-0 to 23b-7, redundancy row address decoders 24b-0 to 24b-7,

15 redundancy ROM circuit groups 28b-0 to 28b-7 each having four redundancy ROM circuits, and a redundancy sub mat decoder 32b. Additionally, the row address X0 to X2 is inputted to a sub word decoder not shown, and a method of selecting words in the memory cell

20 array is the same as that in the first embodiment. Also, word selection with respect to the redundancy memory cell array is the same as in the second embodiment with reference to Fig. 7C, by changing the reference numerals 23a, 24a, and 27a in Fig. 7C to

25 23b, 24b, and 27b, respectively.

The sub mat decoder 31b receives the row address X11 to X13, and outputs the sub mat selection

signals SM0 to SM7 to respective sub mats. The row

address decoders 22b-0 to 22b-7 of respective sub

mats receive the row address X3 to X10, the sub word

decoder receives the row address X0 to X2, and one of

5   the 2048 word lines of each of the memory cell arrays

21b-0 to 21b-7 is activated. The memory cell arrays

21b-0 to 21b-7 of each sub mat are activated by the

corresponding sub mat selection signals SM0 to SM7

from the sub mat decoder 31b, and output data of

10   memory cells that corresponds to one activated word

line. The redundancy sub mat decoder 32b receives

the row address X1 to X13, and outputs eight

redundancy activation signals BE0 to BE7. The eight

redundancy activation signals BE0 to BE7 are

15   connected to the redundancy ROM circuit groups 28b-0

to 28b-7, respectively. The activated redundancy ROM

circuit groups 28b-0 to 28b-7 receive the row address

X4 to X13, and output a comparison result with the

defective address specifying the defective memory

20   cell to the redundancy row address decoder 24b-n as

the redundancy selection signals RE-n-0 to RE-n-3 (n=

0 to 7). The redundancy row address decoder 24b-n

receives the redundancy selection signals RE-n-0 to

RE-n-3, and activates the redundancy main word line

25   RMWD of the redundancy memory cell array 23a-n (n= 0

to 7). One redundancy ROM circuit provided in the

redundancy ROM circuit groups 28b-0 to 28b-7 is

related to two sub word lines of the redundancy memory cell arrays 23b-0 to 23b-7. Therefore, two sub word drivers 29 are connected to one redundancy main word line RMWD. The redundancy memory cell

5 arrays 23b-0 to 23b-7 have four main word lines driven by the redundancy row address decoders 24-0 to 24-7, and output data of the memory cells connected to the sub word line activated by the sub word driver 29.

10   Each of the memory cell arrays 21b-0 to 21b-7 has 2048 word lines, and one word line is selected by the row address decoders 22b-0 to 22b-7 receiving and decoding the row address X0 to X10 and the sub word decoder. When all the redundancy ROM circuits 28b

15 determine that the accessed address does not match the defective address, a relevant memory cell in the memory cell arrays 21b-0 to 21b-7 is accessed. When any of the redundancy ROM circuits 28b determines that the accessed address matches the defective

20 address specifying the defective memory cell, the row address decoder killer signal is activated. Since the row address decoders 22b-0 to 22b-7 are invalidated, the memory cells in the memory cell arrays 21b-0 to 21b-7 is not accessed.

25   The redundancy sub mat decoder 32b decodes the row address X1 to X3, and outputs the eight redundancy activation signals BE0 to BE7. One

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redundancy activation signal BE activates one of the redundancy ROM circuit groups 28b-0 to 28b-7.

Each of the redundancy memory cell arrays 23b-0 to 23b-7 has eight word lines and is a

5 redundancy memory block for replacing the data of the defective address specifying the defective memory cell in the memory cell arrays 21b-0 to 21b-7. The eight word lines of the redundancy ROM circuit group 23b-n correspond in pairs to each of the redundancy

10 selection signals RE-n-0 to RE-n-3 outputted from the redundancy ROM circuit groups 28b-n (n= 0 to 7). The redundancy selection signals RE-n-0 to RE-n-3 each activate one redundancy main word line RMWD by activating the redundancy row address decoder 24b-n

15 (n= 0 to 7). One redundancy main word line RMWD is connected to two sub word drivers 29, and one redundancy sub word line RSWD is selected by the row address X0. The row address X0 is not inputted to the redundancy sub mat decoder 32b, and one

20 redundancy ROM circuit to be activated by the redundancy activation signal BE which is the output of the redundancy sub mat decoder 32b corresponds to two word lines. Therefore, the two word lines correspond to two adjacent word lines of the memory

25 cell arrays 21b-0 to 21b-7.

Here, the relationship between the main word lines and the sub word lines in the memory cell

arrays 21b-0 to 21b-7 has been described in the first embodiment with reference to Fig. 7A. The relationship is the same in the present embodiment as well, and the description thereof is omitted. Also,

5 the relationship between the main word lines and the sub word lines in the redundancy memory cell arrays 23b-0 to 23b-7 is described in the second embodiment with reference to Fig. 7C, by changing the reference numerals 23a, 24a, and 27a in Fig. 7C to 23b, 24b,

10 and 27b respectively. The relationship is the same in the present embodiment as well, and the description thereof is omitted.

An operation when the memory is accessed is explained. If the memory is accessed, the redundancy

15 ROM circuit group 28b-n each having four redundancy ROM circuits 28b-n-0 to 28b-n-3 (n= 0 to 7) compares the defective address specifying the defective memory cell held in the fuses of each of the circuits and the row address X4 to X13 to be inputted. In a case

20 of match, the row address X4 to X13 is determined to be the defective address, and one redundancy selection signal RE is activated. The redundancy main word line that corresponds to the redundancy ROM circuit 28b-n-m (n= 0 to 7, m= 0 to 3) holding the

25 defective address and the sub word line are selected. Then, the redundancy memory cell array 23b-n is activated, and all the memory cell arrays 21b-0 to

21b-7 are inactivated. Therefore, the redundancy memory cell array 23b is accessed instead of the memory cell array 21b, and the defect in the memory cell array 21b is replaced by the redundancy memory

5 cell array 23b. In the case of mismatch, the accessed address is determined not to the defective address specifying the defective memory cell, and the memory cell array 21b is activated and the normal access is performed.

10 Each of the redundancy ROM circuits 28b-0 to 28b-7, when activated by the redundancy activation signals BE0 to BE7 which is obtained by decoding the row address X1 to X3, compares the defective address specifying the defective memory cell held in the fuse

15 and the input row address X4 to X13. Therefore, the row address X1 to X13 is compared with the defective address, and memory cells that belong to two adjacent sub words corresponding to the row address X0 are the target of the replacement (segment).

20 Thus, the segment which is the allocation unit for replacing a defect is two sub memory blocks. In the memory cell array 21b-0 selected by the row address X0 to X10, the memory cell arrays 21b-0-0 and 21b-0-1 are allocated to the redundancy memory cell

25 array 23b-0, the memory cell arrays 21b-0-2 and 21b-0-3 are allocated to the redundancy memory cell array 23b-1, and the memory cell arrays 21b-0-4 and 21b-0-5

are allocated to the redundancy memory cell array

23b-2, in order. Allocation is cyclically performed

in order, where the memory cell arrays 21b-0-14 and

21b-0-15 are allocated to the redundancy memory cell

5   array 23b-7, and the memory cell arrays 21b-0-16 and

21b-0-17 are allocated to the redundancy memory cell

array 23b-0. That is to say, the redundancy memory

cell array 23b-n are recurrently allocated to the

memory cell arrays 21b-0-0 to 21b-0-2047 for every

10   two sub memory blocks in accordance with the row

address X1 to X3 (n= 0 to 7).

Further, the memory cell arrays 21b-i-$(2 \times m)$

and 21b-i-$(2 \times m+1)$ are sequentially allocated to the

redundancy memory cell array 23b-n in the memory cell

15   arrays 21b-1 to 21b-7 as well (i= 1 to 7, m= 0 to

1023, n= 0 to 7, m is the number of segments provided

to the memory cell array, n is given by a reminder

generated when m is divided by eight as the number of

redundancy memory cell arrays which are redundancy

20   memory blocks), as in the case of the memory cell

array 21b-0.

In other words, the following description is

possible. The redundancy memory cell arrays 23b-0 to

23b-7 are provided in correspondence to the memory

25   cell arrays 21b-0 to 21b-7. Each of the memory cell

arrays 21b has 1024 segments of memory array groups

connected to two adjacent sub word lines selected by

the row address X0, as the segment, which is the unit
for the replacement when the defective memory cell is
caused. Based on the row address X1 to X3, the
memory cell array 21b can be considered as a segment
group having eight adjacent segments as a unit, where
one of the segments can be selected. In that idea,
the memory cell array 21b has 128 segment groups
repeatedly arranged that are selected based on the
row address X4 to X10. On the other hand, the sub
mat to which the redundancy memory cell array is
arranged, is selected by the redundancy sub mat
decoder 32b to which the row address X1 to X3 is
inputted. Therefore, eight segments forming the
segment group, and eight sub mats where the
redundancy memory cell arrays are arranged, are
selected by the same row address X1 to X3, having a
correspondence. In other words, the eight segments
are allocated in order, to the redundancy memory cell
arrays arranged in the eight sub mats. Further,
since the eight segments are repeated by the row
address X4 to X10, the eight segments are also
cyclically allocated in order, to the redundancy
memory cell array.

Additionally, the segment n (n= 0 to 1023) is
repeatedly allocated in units of eight, to the same
redundancy memory cell array 23-m (m= 0 to 7).
Therefore, the segment n that satisfies the

relationship of n= 8×A+m, is allocated to the redundancy memory cell array 23-m (m= 0 to 7). Here, A is a value determined by the row address X4 to X10. That is, the segment allocated to the redundancy

5 memory cell array 23-x all has the same segment number specified by the row address X1 to X3.

If such allocation to the redundancy memory cell array is performed, two sub word lines correspond to one redundancy ROM circuit 28b,

10 reducing the number of circuits by half compared with the case of using the redundancy memory cell array having the same capacity. The number of circuits is four in the case of Fig. 11. Further, the row address for comparing the defective address

15 specifying the defective memory cell is X4 to X13, which is less than the comparison address X3 to X13 in the second embodiment by one bit. Consequently, the defect can be repaired while further reducing the fuses for holding the defective address, compared

20 with the second embodiment.

Additionally, in the present embodiment, the segment as the replacement unit for the defective memory cell is the memory cell group connected to two word lines, which is also applicable in extension, to

25 a memory cell group connected to 2^n word lines. Further, the redundancy for the word line (row address) has been described in the present embodiment,

which is obviously applicable to the redundancy for the bit line (column address) as well.

The fourth embodiment is described with reference to Fig. 12. The fourth embodiment is a case where the segment as the unit for a repair by the redundancy circuit, is a memory cell group in a range selected by the main word line. The redundancy memory cell array is driven by one redundancy main word line, and the redundancy memory cell array included in one sub mat repairs one defect. Such a configuration makes it possible to further reduce the number of fuses for holding the defective address specifying the defective memory cell. Here, description is given on the allocation relationship between a memory cell array 21c and a redundancy memory cell array 23c by the row address. Therefore, only a portion relevant to the row address and the memory cell array is shown, and other portions are omitted. Additionally, description is given below on redundancy for the word line (row address), which is obviously applicable to redundancy for the bit line (column address) as well.

A DRAM has memory cell arrays 21c-0 to 21c-7, row address decoders 22c-0 to 22c-7, a sub mat decoder 31c, redundancy memory cell arrays 23c-0 to 23c-7, redundancy row address decoders 24c-0 to 24c-7, redundancy ROM circuits 28c-0 to 28c-7, and a

redundancy sub mat decoder 32c. The memory cell array 21c-n, the row address decoder 22c-n, the redundancy memory cell array 23c-n, the redundancy row address decoder 24b-n, and the redundancy ROM

5   circuit 28c-n are provided to the same sub mat (n= 0 to 7). Additionally, the row address X0 to X2 is inputted to a sub word decoder not shown, and a word selection method of a memory cell array is the same as that in the first embodiment. Also, word

10 selection of a redundancy memory cell array is described in Fig. 7D.

The sub mat decoder 31c receives the row address X11 to X13, and outputs the sub mat selection signals SM0 to SM7 to each sub mat. The row address

15 decoder 22c-0 to 22c-7 of each sub mat receives the row address X3 to X10, and receives the row address X0 to X2 to the sub word decoder, activating one of the 2048 word lines of each of the memory cell arrays 21c-0 to 21c-7. The memory cell arrays 21c-0 to 21c-

20 7 of each sub mat are activated by the corresponding sub mat selection signals SM0 to SM7 from the sub mat decoder 31c, and output data of a memory cell that corresponds to one activated word line among the 2048 word lines selected by the row address decoder 22c-0

25 to 22c-7, and the sub word decoder. The redundancy sub mat decoder 32c receives the row address X3 to X5, and outputs eight redundancy activation signals BE0

to BE7. The eight redundancy activation signals BE0
to BE7 are connected to the redundancy ROM circuits
28c-0 to 28c-7 respectively. Therefore, the
redundancy ROM circuit 28c is selected by the row

5 address X3 to X5, to then be activated. The
redundancy ROM circuits 28c-0 to 28c-7 receive the
row address X6 to X13, and output a comparison result
with the defective address specifying the defective
memory cell, to the redundancy row address decoder

10 24c-n (n= 0 to 7), as the redundancy selection signal
RE-n. The redundancy row address decoder 24c-n
receives the redundancy selection signal RE-n, and
activates the redundancy main word line RMWD of the
redundancy memory cell array 23c-n (n= 0 to 7). Each

15 of the redundancy ROM circuits 28c-0 to 28c-7
corresponds to eight sub word lines included in each
of the redundancy memory cell arrays 23c-0 to 23c-7.
Therefore, one redundancy main word line RMWD is
connected to eight sub word drivers 29. Each of the

20 redundancy memory cell arrays 23c-0 to 23c-7 has one
main word line driven by the corresponding redundancy
row address decoders 24c-0 to 24c-7, and outputs the
data of the memory cell connected to the sub word
line activated by the sub word driver 29.

25   The memory cell arrays 21c-0 to 21c-7 are
each provided with 2048 word lines that are selected
by decoding the row address X0 to X10 by using the

row address decoder 22c-0 to 22c-7 and the sub word decoder. When all the redundancy ROM circuits 28c judge that the accessed address does not correspond to the defective address, the memory cell arrays 21c-0 to 21c-7 have a relevant memory cell to be accessed. If any of the redundancy ROM circuits 28c judges that the accessed address corresponds to the defective address, the row address decoder killer signal is activated, and the row address decoders 22c-0 to 22c-7 get invalid. Therefore, the memory cell of the memory cell arrays 21c-0 to 21c-7 is not accessed.

The redundancy sub mat decoder 32c receives and decodes the row address X3 to X5, and outputs the eight redundancy activation signals BE0 to BE7 to the redundancy ROM circuits 28c-0 to 28c-7. Therefore, the redundancy ROM circuits 28c-0 to 28c-7 are selected based on the row address X3 to X5, to then be activated.

The redundancy memory cell arrays 23c-0 to 23c-7 each having eight word lines, are redundancy memory blocks for replacing the data of the defective address specifying the defective memory cell of the memory cell arrays 21c-0 to 21c-7. Eight word lines of the redundancy memory cell array 23c-n correspond to the redundancy selection signal RE-n outputted from the redundancy ROM circuit 28c-n. The redundancy selection signal RE-n each activates one

redundancy main word line RMWD by the redundancy row address decoder 24c-n. One redundancy main word line RMWD is connected to eight sub word drivers 29, and one redundancy sub word line RSWD is selected by the

5 row address X0 to X2. Since the row address X0 to X2 showing the address of the sub word is not inputted to the redundancy sub mat decoder 32c, eight word lines to be activated correspond to the main word line MWD of the memory cell arrays 21c-0 to 21c-7.

10 Here, description is given on the relationship between the main word line and the sub word line in the redundancy memory cell arrays 23c-0 to 23c-7, and on the allocation relationship between the sub memory block of the memory cell arrays 21c-0

15 to 21c-7 having a defect, and the redundancy sub memory block of the redundancy memory cell arrays 23c-0 to 23c-7 for replacing the former. The relationship between the main word line and the sub word line in the memory cell arrays 21c-0 to 21c-7

20 was described in the first embodiment with reference to Fig. 7A. The relationship is the same in the present embodiment as well, and the description thereof is omitted. The relationship between the main word line and the sub word line in the

25 redundancy memory cell arrays 23c-0 to 23c-7 is explained with reference to Fig. 7D. Fig. 7D shows the redundancy memory cell array 23c-0 in the sub mat

17-0, and relevant redundancy row address decoder 24c-0, sub word decoder 27c-0, sense amplifier 25-0, and column address decoder 18.

The redundancy row address decoder 24c-0 5 receives the redundancy selection signal RE-0, and activates one redundancy main word line RMWD that corresponds to the redundancy selection signal RE-0. The sub word decoder 27c-0 outputs eight decode signals activated based on the row address X0 to X2. 10 In the redundancy memory array 23c-0, the sub word driver 29 activates the redundancy sub word line RSWD based on the activated decode signal and the redundancy main word line RMWD, and activates the sub memory block 35, which is the memory cell group 15 connected to the redundancy sub word line RSWD. The sense amplifier 25-0 is selected by the column address decoder 18 based on the column address, data stored in the memory cell activated by the sense amplifier 25-0 is read, and data inputted from the 20 outside is written.

The sub word decoder 27c-0 outputs eight decode signals activated based on the row address X0 to X2. The sub word drivers 29-0 to 29-7 are arranged at intersection points of the decode signal 25 line and the redundancy main word line. The sub word drivers 29-0 to 29-7 each activate one redundancy sub word line RSWD based on the redundancy main word line

RMWD and the decode signal. Since the sub word

drivers 29-0 to 29-7 correspond to eight decode

signals of the sub word decoder 27c-0 respectively,

the sub word drivers 29-0 to 29-7 receive the decode

5 signals activated when the row address X0 to X2 is

"0" to "7". Such connection makes it possible to

specify the sub memory block in the segment. The

same connection is performed to other sub mats as

well.

10   Additionally, in such connection, the segment,

which is the allocation unit for repairing the defect

of the memory cell array by using the redundancy

memory array, is eight sub memory blocks. Therefore,

the sub memory blocks 35-0 to 35-7 are allocated as

15 the redundancy segment 26, serving as the memory

array for replacing the defect generated in eight

adjacent sub words (one main word) of the memory

arrays 21-0 to 21-7. The allocated redundancy

segment repairs the defect by replacing each one sub

20 memory block of the memory cell arrays 21c-0 to 21c-7

having the defect and being accessed.

           An operation when the memory is accessed is

described. If the memory is accessed, the redundancy

ROM circuits 28c-0 to 28c-7 activated by an output

25 signal of the redundancy sub mat decoder 32c receive

the row address X6 to X13, and compare the inputted

row address X6 to X13 with the defective address

specifying the defective memory cell of the memory
cell array 21c-0 to 21c-7 held in the fuse provided
inside. In the case of match as a result of the
comparison, the input row address X6 to X13 is
5   regarded as the defective address specifying the
defective memory cell, the redundancy selection
signal RE being activated. The redundancy row
address decoder 24c-n to which the activated
redundancy selection signal RE is supplied, activates
10 the redundancy main word line RMWD. Then, the
redundancy main word line that corresponds to the
redundancy ROM circuit 28c-n holding the corresponded
address, and the sub word line are selected, and the
redundancy memory cell array 23c-n is activated. In
15 addition to the activation of the redundancy memory
cell array 23c-n, all the memory cell arrays 21c-0 to
21c-7 are inactivated by the row address decoder
killer signal. Therefore, the redundancy memory cell
array 23c is accessed instead of the memory array 21c,
20 and the defect of the memory cell array 21c is
replaced by using the redundancy memory cell array
23c. In the case of mismatch as a result of the
comparison, the accessed address is regarded not to
be the defective address specifying the defective
25 memory cell, and the memory cell array 21c is
activated and normal access is performed.

Each of the redundancy ROM circuits 28c-0 to

28c-7, when activated by the redundancy activation signals BE0 to BE7 which is obtained by decoding the row address X3 to X5, compares the defective address specifying the defective memory cell held in the

5 fuses with the input row address X6 to X13. Therefore, the row address X3 to X13 is compared with the defective address, and a memory cell that belongs to one main word that includes eight sub words corresponding to the row address X0 to X2 is the

10 object of replacement (segment).

Thus, the segment as the allocation unit for replacing the defect is eight sub memory blocks (corresponding to the main word). In the memory cell array 21c-0 selected by the row address X0 to X10,

15 the memory cell arrays 21c-0-0 to 21c-0-7 are allocated to the redundancy memory cell array 23c-0, the memory cell arrays 21c-0-8 to 21c-0-15 are allocated to the redundancy memory cell array 23c-1, and the memory cell arrays 21c-0-16 to 21c-0-23 are

20 allocated to the redundancy memory cell array 23c-2 sequentially. Further, the allocation is cyclically performed in order, where the memory cell arrays 21c-0-56 to 21c-0-63 are allocated to the redundancy memory cell array 23c-7, and then the memory cell

25 arrays 21c-0-64 to 21c-0-71 are allocated to the redundancy memory cell array 23c-n.

Further, the memory cell array 21c-i-(8m) to

21c-i-(8m+7) are allocated in order, to the redundancy memory cell array 23c-n in the memory cell arrays 21c-1 to 21c-7 as well, as in the case of the memory cell array 21c-0 (m= 0 to 255, n= 0 to 7, m is

5 the number of segments provided to the memory cell array, n is given by a reminder obtained when m is divided by eight which the number of redundancy memory blocks).

If such allocation to the redundancy memory

10 cell array is performed, one redundancy ROM circuit 28c corresponds to eight sub word lines, namely one main word line, the number of circuits being one-eighth compared with the case where a redundancy memory cell array with the same capacity is used. In

15 Fig. 12, eight sub words are used for one circuit. Also, since the defective address specifying the defective memory cell to be held in the redundancy ROM circuit 28c has only eight bits, which are X6 to X13, the number of fuses per circuit can also be

20 reduced. Therefore, reduction in the number of circuits and in the number of fuses per circuit makes it possible to greatly reduce the number of fuses per memory chip and repair the defect. In addition, if the capacity of the redundancy memory array 23c is

25 increased, the present embodiment can be extended and applied to a plurality of main word lines.

The redundancy circuit of the row side has

been described in the above embodiments for

simplification of explanation, which is clearly

applicable to the redundancy circuit of the column

side as in the case of the row side, if the segment

5   is read as a memory cell group connected to the same

bit line and a plurality of adjacent bit lines.

Further, description has been made on the allocation

of the redundancy memory block with an example of the

DRAM.   However, it is clear that the present

10 invention can be applicable not only to the DRAM but

also to a memory having a redundancy memory.

Brief Description of Drawings

Fig. 1A is a diagram showing a relationship

15 between a defective segment and a redundancy memory

block according to a conventional technique;

Fig. 1B is a diagram showing a relationship

between defective segments and a redundancy memory

block according to a conventional technique;

20   Fig. 2 is a block diagram showing a

configuration of a MAT in the conventional technique;

Fig. 3 is a block diagram showing a

configuration of a portion of an extended redundancy

ROM circuit according to the conventional technique;

25   Fig. 4 is a block diagram showing a

configuration of a DRAM according to a first

embodiment of the present invention;

Fig. 5 is a block diagram showing a configuration of a MAT according to the first embodiment of the present invention;

Fig. 6 is a block diagram showing a

5　configuration of a redundancy ROM circuit according to the first embodiment of the present invention;

Fig. 7A is a block diagram showing a relationship between a main word line MWD and a sub word line SWD in a memory cell array according to the

10　first embodiment of the present invention;

Fig. 7B is a block diagram showing a relationship between a main word line MWD and a sub word line SWD in a redundancy memory cell array according to the first embodiment of the present

15　invention;

Fig. 7C is a block diagram showing a relationship between a main word line MWD and a sub word line SWD in a redundancy memory cell array according to second and third embodiments of the

20　present invention;

Fig. 7D is a block diagram showing a relationship between a main word line MWD and a sub word line SWD in a redundancy memory cell array according to a fourth embodiment of the present

25　invention;

Fig. 8 is a timing chart showing an operation waveform according to the first embodiment of the

present invention;

Fig. 9 is a diagram showing a relationship between a sub word and a redundancy ROM circuit according to the present invention;

5   Fig. 10 is a block diagram showing a configuration of the second embodiment according to the present invention;

Fig. 11 is a block diagram showing a configuration of the third embodiment according to

10   the present invention; and

Fig. 12 is a block diagram showing a configuration of the fourth embodiment according to the present invention.